## REMARKS

Claims 13, 15-17, 19 and 20 are rejected under 35 USC §103 as obvious over Mizuno et al., US Patent 6,077,757 in view of Morishima, US Patent Publication 20010011857.

Independent claim 13 recites a second substrate closely adhered to the other face of the sealing wall. Likewise, the second substrate has a plurality of openings at sites confronting the plurality of electrode pads.

Mizuno et al. '757 describes a method of fabricating a chip semiconductor device includes steps in which electrically conductive bumps are provided on electrodes of semiconductor elements on a wafer. An insulating substrate has an electrode pattern is combined onto the wafer so that the electrode pattern is made into contact with the bumps. Only the wafer on which the semiconductor elements are provided is divided by grooves into a plurality of chips each of which has a semiconductor element. A liquid resin is flowed into the grooves and onto the chips for subsequent curing the resin, and the cured resin and the insulating substrate are concurrently cut along the grooves so that a plurality of semiconductor devices are formed.

Morshima '857 describes a surface acoustic wave device that is small, lightweight, and highly reliable, and protects its functional portion. The surface acoustic wave device has surface acoustic wave elements mounted on a circuit substrate. Each substrate acoustic wave element includes a frame like first insulating film furnished to surround functional portions on a chip. A lid-like second insulating film is deposited on the first insulating film so as to cover

driving electrodes and surface wave propagation paths of the functional portions, while securing a hollow portion over the functional portions.

Mizuno et al. '757 does not describe a sealing wall being configured to enclose the electronic circuit device with the electrode pad arranged outside of the sealing wall as indicated by the Examiner and recited in claim 13. According to the manufacturing method described in the present application, an electronic circuit device ignored on one main surface of the first substrate is sealed by the sealing wall and a second substrate, which can prevent the electronic circuit device from a detrimental effect exerted by a process carried out after sealing to form an electrically conductive member on an electrode pad.

Mizuno et al. '757 contains no description or suggestion that the process of forming the electrically conductive member on the electrode pad (depicted in Fig. 7C) could have a detrimental effect on the electronic circuit device. Therefore, any assertion that a person skilled in the art can easily achieve the invention of this application by applying the technique of forming insulating films 2a and 2b before formation of the bump electrode 6 described by Morishita '857 to the invention disclosed by Mizuno et al. '757 is clearly erroneous.

In addition to failing to describe the sealing wall of the present invention, Mizuno et al. '757 does not describe a manufacturing process such as a method according to the invention of this application in which, after closely adhering the sealing walls to one main surface of the first substrate and then closely adhering the second substrate which has a plurality of openings to the sealing wall (the first step), the electrically conductive member is formed on the electrode pads (the second step). In the embodiment depicted in Fig. 4A-4F of Mizuno et al.

'757, a method in which a second substrate having grooves 7 is bonded after forming metal bumps on a first substrate (corresponding to the step of forming the electrically conductive member) is described, whereas a method in which via holes 19 are formed in the second substrate (Fig. 7B) after bonding the second substrate 18 having no opening to the semiconductor wafer (the first substrate) (Fig. 7A) is described in the embodiment depicted in Figs. 7A-7F. It is apparent that the method described in the embodiment of Figs- 4A-4F in Mizuno et al. '757 cannot be applied in combination with the method described in the embodiment of Fig. 7A-7F, and there is no description and no suggestion regarding the possibility of implementing the two methods at the same time in the Mizuno et al. '757 citation

Moreover, Morishima '857 does not teach or suggest a second substrate having a plurality of openings at sites where bonding occurs, as stated by the Examiner.

Thus, the combination of Mizuno et al. '757 and Morishima '857 does not render obvious independent claim 13.

As to claims 15-17, 19 and 20, they are dependent on claim 13, respectively. Therefore, claims 15-17, 19 and 20 are also allowable for the same reasons argued with respect to claim 13.

In view of the above amendments and for all the reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw the objections and rejection made under 35 U.S.C. §§ 103 and 112, second paragraph. Accordingly, an early indication of allowability is earnestly solicited.

If the Examiner has any questions regarding matters pending in this application, please feel free to contact the undersigned below.

Respectfully submitted,

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